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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,701	06/24/2003	Ching-Fa Yeh	BHT-3230-56	7550

7590 05/25/2005

TROXELL LAW OFFICE PLLC
SUITE 1404
5205 LEESBURG PIKE
FALLS CHURCH, VA 22041

EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,701	YEH ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 3/3/05. Currently, claims 8-14 are pending.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the active layer must be shown, specifically in figures 1-3 or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: On page 5, lines 9, "etc.." should be "etc.". In addition, on line 14, "15by" should be "15 by". Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are: For example, on page 4, lines 22-24, "d) process, a thermal insulating layer of laser annealing or a hard mask of the removal pf polysilicon spacer after recrystallization;" is unclear in its meaning. In addition, on page 4, lines 25-28, "using a solution of silicon dioxide 6 of wet isotropic etching..." How is this possible? Especially since conventionally wet etching techniques may be used to etch silicon dioxide. Finally, on pages 5-6, lines 10-11, 21-22 and 1-3, respectively, "the polysilicon spacer 7" is disclosed as being "behind either side of the active layer", "under either side of the active layer" and "to be surrounded the side of active layer" it is unclear what is the meaning with regards to the location of the "polysilicon spacer 7". According the disclosed figures 1-3, it appears that the "polysilicon spacer 7" is on either side of

"the amorphous silicon layer 3", however, it is unclear what direction exactly where is the active layer, etc. Clarification is requested.

In general, the Examiner takes to position that the newly revised specifications and the claims, still lacks clarity with regards to the disclosure of the claimed invention, in addition, includes numerous grammar and spelling errors.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is indefinite, with regards to claim 8, line 10, whether the silicon dioxide is included in the solution for wet isotropic etching. How is this possible? Especially since conventionally wet etching techniques may be used to etch silicon dioxide. Clarification is requested.

Claim 8-14 recites the limitation "forming a hard mask being a photoresist on the low temperature polycrystalline silicon thin film..."" in lines 7-8. There is insufficient antecedent basis for this limitation in the claim.

Claim 8-14 recites the limitation "...thereby protecting the polysilicon spacer from removal" in lines 22-23. There is insufficient antecedent basis for this limitation in the claim.

Claim 11 recites the limitation "wherein the forming step i)..." in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato et al. US Patent 5,589,406 in view of Hasegawa Patent Application Publication US 2004/0026738, in so far as the Examiner can interpret the disclosure and claimed invention.

Kato discloses the semiconductor method substantially as claimed. See figures 1-7 especially, Table 1, and corresponding text, where Kato teaches a method for fabrication of polycrystalline silicon thin film transistors, pertaining to claim 8, comprising the steps of: a) selecting a substrate **100** b) forming a buffer oxide (Table 1; col. 11, lines 1-8, insulating substrate) on the substrate; c) depositing a first amorphous silicon film (1 in Table 1) on the buffer oxide (col. 7, lines 55-67; col. 10, lines 56-67; col. 11, lines 1-31); d) depositing a low-temperature oxide (4 in Table 1) on the first amorphous silicon film (col. 10, lines 56-67; col. 11, lines 1-31); e) forming a hard mask being a photoresist on the low temperature polycrystalline silicon thin film transistor (LTPS-TFT) as an active layer (col. 10, lines 56-67; col. 11, lines 1-31); f) etching the buffer oxide utilizing a solution of silicon dioxide for wet isotropic etching (col. 10, lines 56-67; col. 11, lines 1-31); i) forming large silicon grain structures in the active layer by annealing and recrystallization of an dog-bone shaped portion of the active layer utilizing on of a high-energy continuous wavelength laser and an excimer laser, wherein the low temperature oxide being a stop layer for the first amorphous silicon film during the dry etching

process, and a thermal insulating layer and a hard mask for the first amorphous silicon film during laser annealing (figure 5; col. 10, lines 1-33). In addition, Kato teaches, pertaining to claim 11, wherein the forming step i) the annealing is performed utilizing a method selected from a group consisting of excimer laser annealing (ELA), solid phase crystallization (SPC) and metal-induced lateral crystallization (MILC), and the polysilicon spacer being on opposing sides to the active layer (col. 1, lines 65-67; and col. 2, lines 1-48; col. 9, lines 49-67). Also, Kato shows, pertaining to claim 13, wherein the etching step f) is performed before the removal of said hard mask (col. 10, lines 56-67; col. 11, lines 1-31). Finally, Kato shows, pertaining to claim 14, wherein the etching step f) is performed after the removal of said hard mask (col. 10, lines 56-67; col. 11, lines 1-31).

However, Kato fails to show, pertaining to claim 8, g) depositing a second amorphous silicon film on the active layer; h) forming a poysilicon spacer by dry etching behind either said of the active layer of the low temperature polycrystalline silicon thin film transistor (LTPS-TFT) and i) forming large silicon grain structures in the active layer by annealing and recrystallization of an dog-bone shaped portion of the active layer utilizing on of a high-energy continuous wavelength laser and an excimer laser, wherein the low temperature oxide being a stop layer for the first amorphous silicon film during the dry etching process, and a thermal insulating layer and a hard mask for the first amorphous silicon film during laser annealing thereby protecting the poly silicon spacer from removal. In addition, Kato fails to show, pertaining to claim 9, wherein the polysilicon spacer is selected from the group consisting of polycrystalline silicon film and amorphous silicon film. Also, Kato fails to show, pertaining to claim 10, wherein the polysilicon spacer of the forming step h) is formed on form two opposing

sides of the active layer, the active layer is selected from a group consisting of a thin film transistor (TFT) and silicon-on-insulator metal oxide semiconductor field effect transistor (SOI-MOSFET) in one of a low temperature and a high temperature process. Kato fails to show, pertaining to claim 12, wherein the polysilicon spacer of the forming step h) generates a temperature gradient.

Hasegawa teaches, in figures 1-7, and corresponding text, a polycrystalline CMOS device, that includes the use of a second polycrystalline silicon, formed on a silicon active layer to create side spacers for the active layer (figures 5A-5E; paragraphs [0040-0041]).

It would have been obvious to one of ordinary skill in the art to substitute the following steps: g) depositing a second amorphous silicon film on the active layer; h) forming a poysilicon spacer by dry etching behind either said of the active layer of the low temperature polycrystalline silicon thin film transistor (LTPS-TFT) and i) forming large silicon grain structures in the active layer by annealing and recrystallization of an dog-bone shaped portion of the active layer utilizing on of a high-energy continuous wavelength laser and an excimer laser, wherein the low temperature oxide being a stop layer for the first amorphous silicon film during the dry etching process, and a thermal insulating layer and a hard mask for the first amorphous silicon film during laser annealing thereby protecting the poly silicon spacer from removal; wherein the polysilicon spacer is selected from the group consisting of polycrystalline silicon film and amorphous silicon film; wherein the polysilicon spacer of the forming step h) is formed on form two opposing sides of the active layer, the active layer is selected from a group consisting of a thin film transistor (TFT) and silicon-on-insulator metal oxide semiconductor field effect transistor (SOI-MOSFET) in one of a low temperature and a high temperature process; wherein

the polysilicon spacer of the forming step h) generates a temperature gradient, in the method of Kato, pertaining to claims 8, 9, 10 and 12, according to the teachings of Hasegawa, with the motivation, that, the resistance depends on the crystal grain diameter, grain boundaries and on film thickness, of the polycrystalline silicon. Therefore, it would be obvious to one of ordinary skill in the art use a polysilicon spacer formed on the on the active layer, for the purpose of adjusting the crystal grain diameter and grain boundaries of the active layer of a low temperature polycrystalline silicon thin film transistor (LTPS-TFT). In addition, it would be obvious to form large silicon grain structures of the active layer by recrystallizing with a high-energy continuous wavelength laser or with an excimer laser annealing on a dog-bone shape active layer, resulting in a uniform crystal grain diameter and grain boundaries on the active layers, for the purpose of eliminating current leakage, resulting in a more efficient semiconductor device. Also, it would have been obvious to substitute the polysilicon spacer with for example, a dielectric material containing an oxide, to possibly reduce the active layer region thus creating an additional isolation between of active layers of additional semiconductor devices.

Response to Arguments

Applicant's arguments filed 3/3/05 have been fully considered but they are not persuasive. In response to the Applicant's Remarks, pages 8-11:

Applicant raises the clear issue of whether Kato taken alone or, the combination of Kato in view of Hasegawa, teaches the following steps: "depositing a second amorphous silicon film on the active layer; forming a polysilicon spacer by dry-etching behind either side of the active layer of the low temperature polysilicon thin film transistor (LTPS-TFT); forming large silicon

grain structures in the active layer by annealing and recrystallization of an dog-bone shaped portion of the active layer utilizing one of a high-energy continuous wavelength laser and an excimer laser". In addition, the Applicant raises the clear issue of whether Kato taken alone or, the combination of Kato in view of Hasegawa, teaches, "depositing a low-temperature oxide on the first amorphous silicon; film forming a hard mask being a photoresist on the low temperature polycrystalline silicon thin film transistor (LTPS-TFT) as an active layer."

The Examiner takes to position that the newly revised specifications and the claims, still lacks clarity with regards to the disclosure of the claimed invention, in addition, includes numerous grammar and spelling errors. Therefore, the rejection is based on as far as can be interpreted, since the Applicant fails to clearly disclose the claimed invention. However, for the sake of *arguendo*, the method for fabrication of polycrystalline silicon thin film transistors, with regard to the active layer, as shown by Kato (figures 1-14), and the implications (figure 5; col. 10, lines 1-33), taken in combination with the solid teachings of Jang, would lead one of ordinary skill in the art to have added the second polycrystalline spacer taught by Jang, to the active layer of the Kato.

Kato teaches, in general a polycrystalline silicon active layer used for a thin film transistor device, where theses active layers are formed into dog-bone islands on an insulated substrate. Also, Kato teaches that the crystallization of this polycrystalline silicon active layer is performed by the use of conventional laser annealing techniques that includes an excimer laser. It takes the disclosure of Hasegawa, to describe the improvement of including a polycrystalline spacer. One of ordinary skill in the art would find it possible to add the polycrystalline spacer, as taught by Hasegawa, for the purpose of adjusting the crystal grain diameter and grain boundaries

of the active layer resulting in a uniform crystal grain diameter and grain boundaries on the active layers, and to further eliminating current leakage, resulting in a more efficient semiconductor device.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
May 15, 2005

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER

IN THE DRAWINGS:

Enclosed are new formal drawings of Figures 1-7, accompanied by a LETTER TO THE OFFICIAL DRAFTSPERSON. Figure 1 was amended to correct the reference line for reference number "6",and the words "Wet Etching" were deleted.. Figure 2 was amended to properly identify reference line with reference numbers "1", "2", "3", "3a", "4", "7", and "8", and the words "Dry Etching" were deleted. Figure 3 was amended to add reference number "15", and the words "Excimer Laser Recrystallization" and "Direction of Grain Growth" were deleted. Figure 4 was amended to replace the words with reference numbers --7--, --10--, --11--, and --12--. Figure 5 was amended to replace the words with reference number --7--. Figure 6 was amended to replace the words with reference numbers --7--, --13--, and --14--. Figure 7 was amended to replace the words with reference numbers --7--, --10--, --11--, and --12--, and add the label --Prior Art--.

REPLACEMENT SHEET DRAWING

Please
Enter
SDF 5/17/05

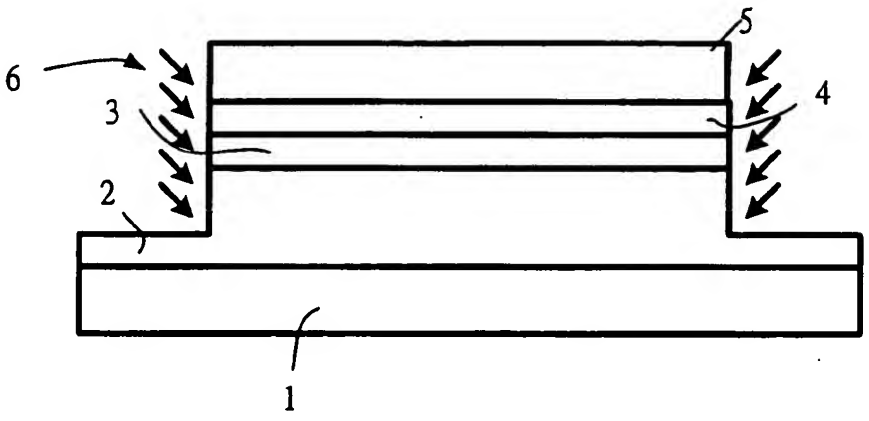

FIG. 1

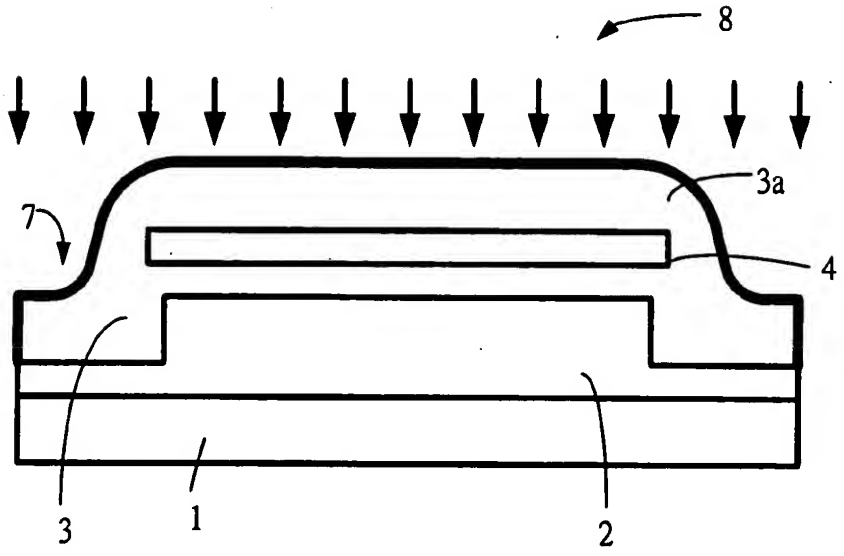

FIG. 2

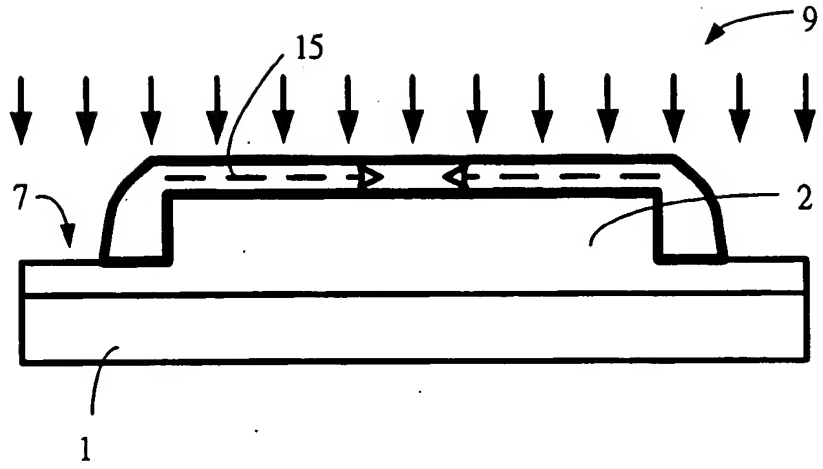

FIG. 3

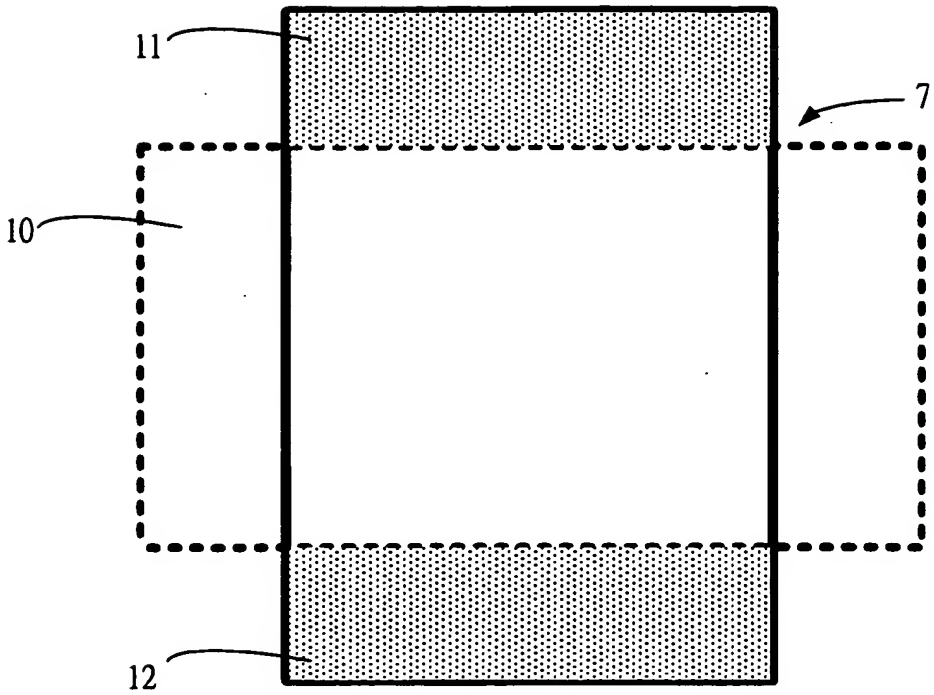

FIG. 4

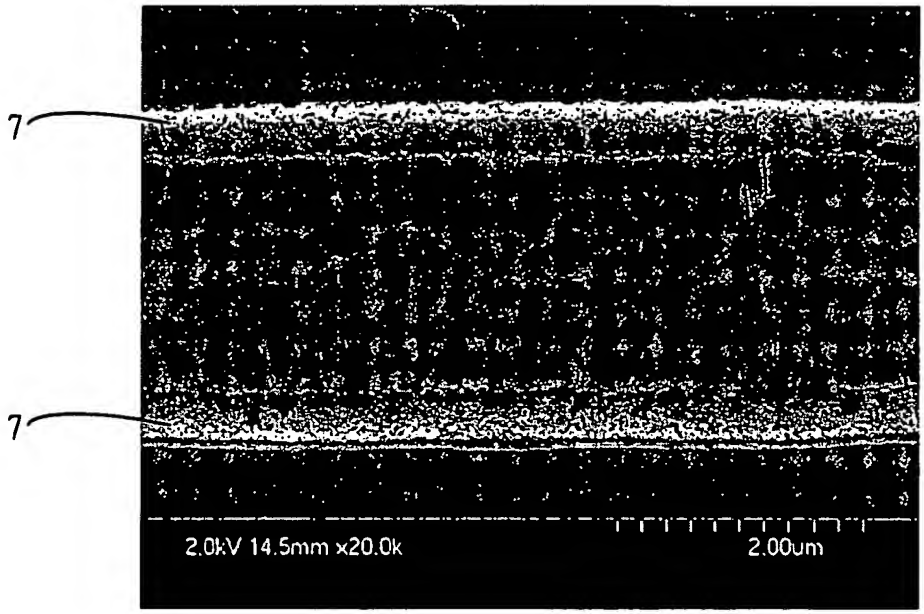

FIG. 5

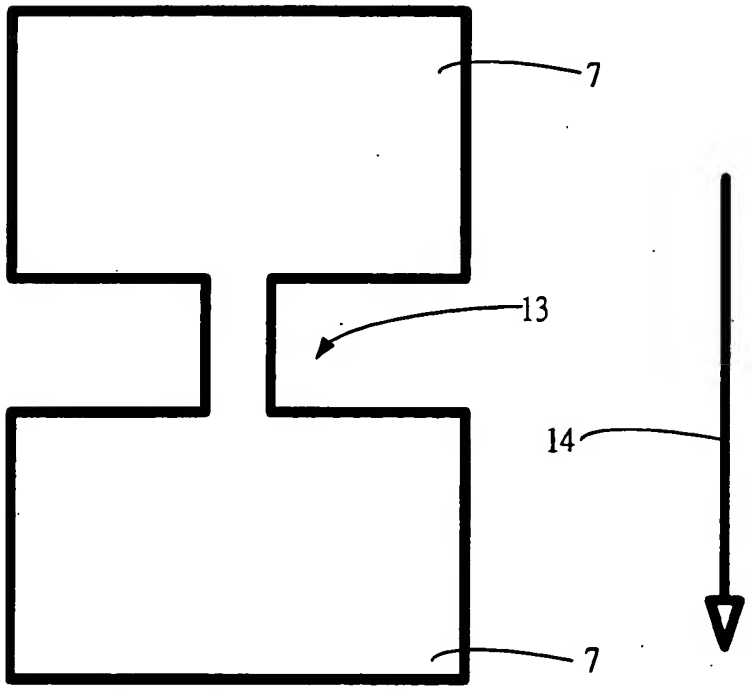

FIG. 6

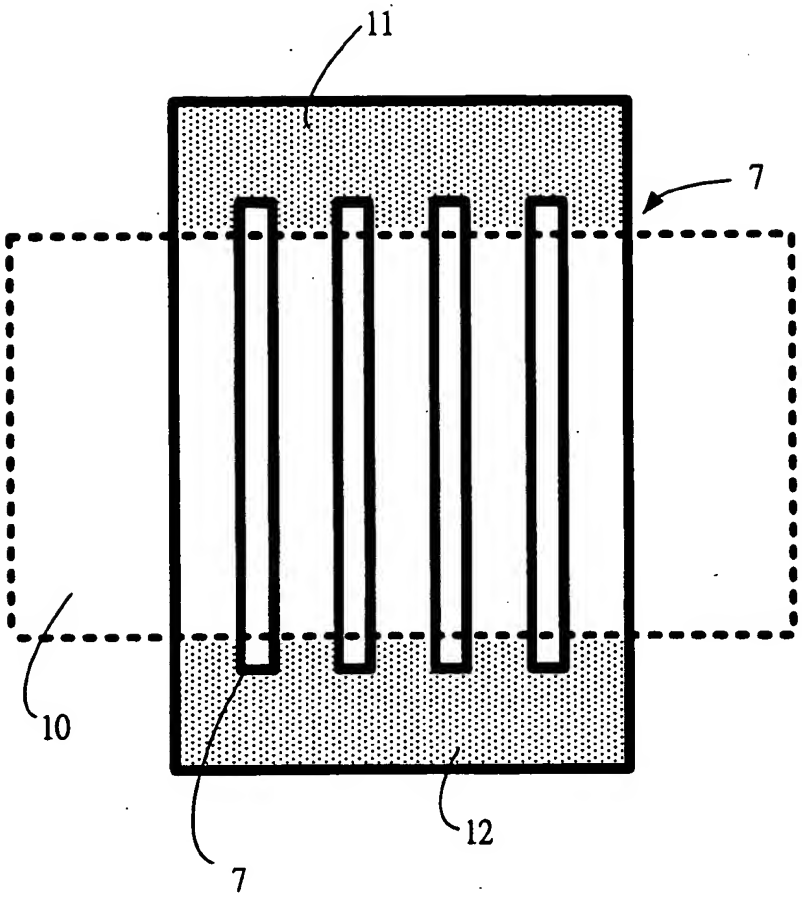

FIG. 7
(Prior Art)